

WHAT IS CLAIMED IS:

1 1. A circuit for providing an indication that a signal level of a primary power
2 source transitions below a predefined threshold level, the circuit comprising:

3 a first transistor electrically coupled to a second transistor, a common node
4 being formed along the coupling;

5 a third transistor having a gate terminal coupled to the common node; and

6 at least one pair of series connected trimming transistors, a first transistor of
7 the at least one pair of trimming transistors having a gate terminal coupled to the common
8 node, the at least one pair of series connected trimming transistors coupled to a drain/source
9 region of the third transistor.

 2. The circuit according to claim 1, further including a fuse electrically coupled to
a gate terminal of a second transistor of the at least one pair of trimming transistors, the fuse
being blown to selectively turn on/off the second transistor of the at least one pair of trimming
transistors.

1 3. The circuit according to claim 1, wherein the first transistor is coupled to the
2 primary power source and a gate terminal of the second transistor is coupled to a substrate of
3 the circuit.

1 4. A circuit, comprising:
2 a first transistor having its source/drain terminals connected between a external
3 power supply voltage and a first node;
4 a second transistor having its source/drain terminals connected between the
5 first node and a reference voltage, and further having a gate terminal connected to receive a
6 substrate voltage related to a backup supply voltage; and
7 a third transistor having its source/drain terminals connected between an output
8 node and the reference voltage, and further having a gate terminal connected to the first node.

1 5. The circuit of claim 4 wherein the first transistor is a p-channel device and the
2 second and third transistors are n-channel devices.

1 6. The circuit of claim 4 wherein the third transistor drives the output node to
2 change state responsive to a drop in the external power supply voltage below a threshold
3 value.

1 7. The circuit of claim 6 wherein the threshold value depends on a pull exerted by
2 the first transistor.

1 8. The circuit of claim 7 further including circuitry for adjusting the pull exerted
2 by the first transistor to effectuate a change in the threshold value.

1 9. The circuit of claim 8 wherein the circuitry comprises a pair of drain/source
2 terminal series connected transistors which are connected between the external power supply
3 voltage and the output node, a first one of the pair of transistors having its gate terminal
4 connected to the first node and a second one of the pair of transistors having its gate terminal
5 connected to receive a threshold voltage trim control signal.

1 10. The circuit of claim 8 wherein the circuitry comprises a plurality of pairs of
2 drain/source terminal series connected transistors, each pair being connected between the
3 external power supply voltage and the output node, a first one of the transistors in each pair
4 having its gate terminal connected to the first node and a gate terminal of each second one of
5 the transistors in each pair connected to receive its own threshold voltage trim control signal.

1 11. The circuit of claim 10 wherein a first subset of the plurality of pairs receive
2 voltage trim control signals to drive the second transistors in each pair to a normally on
3 condition and a second subset of the plurality of pairs receive voltage trim control signals to
4 drive the second transistors in each pair to a normally off condition.

1 12. The circuit of claim 11 further including a trim selection circuit operable to
2 selectively and individually configure the voltage trim control signals to change the normally
3 on/off condition of the second transistors in each pair.

1 13. The circuit of claim 12 wherein the trim selection circuit comprises selectively
2 blowable fuse circuitry.

1 14. The circuit of claim 4 further including pull up circuitry connected between the
2 external power supply voltage and the output node.

1 15. The circuit of claim 14 wherein the pull up circuitry comprises a pair of
2 drain/source terminal series connected transistors which are connected between the external
3 power supply voltage and the output node, a first one of the pair of transistors having its gate
4 terminal connected to the first node and a second one of the pair of transistors having its gate
5 terminal connected to the reference voltage.

1 16. A circuit for providing an indication that a voltage of a primary power source
2 transitions below a threshold level, comprising:

3 a first transistor;

4 a second transistor electrically coupled to the first transistor at a common node;

5 a third transistor having a gate terminal coupled to the common node and a
6 conduction terminal at which the indication is produced; and

7 a pair of series connected threshold level trimming transistors, a first transistor
8 of the pair having a gate terminal coupled to the common node, a second transistor of the pair
9 receiving a threshold level trimming control signal, and the pair being coupled to the
10 conduction terminal at which the indication is produced.

1 17. The circuit of claim 16, wherein the first transistor is coupled to the primary
2 power source and a gate terminal of the second transistor is coupled to a substrate of the
3 circuit.

1 18. The circuit of claim 16 wherein the first transistor exerts a pull which sets the
2 threshold level, the pair of series connected threshold level trimming transistors adjusting the
3 pull exerted by the first transistor in response to the threshold level trimming control signal to
4 effectuate a change in the threshold level.

1 19. The circuit of claim 16 further including pull up circuitry connected between
2 the external power supply voltage and the conduction terminal at which the indication is
3 produced.

1 20. The circuit of claim 19 wherein the pull up circuitry comprises a pair of
2 drain/source terminal series connected transistors which are connected between the external
3 power supply voltage and the conduction terminal at which the indication is produced, a first
4 one of the pair of transistors having its gate terminal connected to the first node and a second
5 one of the pair of transistors having its gate terminal connected to the reference voltage.